Nanometer-Scale Oxide Thin Film Transistor with Potential for High-Density Image Sensor Applications

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ABSTRACT The integration of electronically active oxide components onto silicon circuits represents an innovative approach to improving the functionality of novel devices. Like most semiconductor devices, complementary-metal-oxide-semiconductor image sensors (CISs) have physical limitations when progressively scaled down to extremely small dimensions. In this paper, we propose a novel hybrid CIS architecture that is based on the combination of nanometer-scale amorphous In−Ga−Zn−O (*a*-IGZO) thin-film transistors (TFTs) and a conventional Si photo diode (PD). With this approach, we aim to overcome the loss of quantum efficiency and image quality due to the continuous miniaturization of PDs. Specifically, the *a*-IGZO TFT with 180 nm gate length is probed to exhibit remarkable performance including low 1/*f* noise and high output gain, despite fabrication temperatures as low as 200 °C. In particular, excellent device performance is achieved using a double-layer gate dielectric (Al_2O_3/SiO_2) combined with a trapezoidal active region formed by a tailored etching process. A self-aligned top gate structure is adopted to ensure low parasitic capacitance. Lastly, three-dimensional (3D) process simulation tools are employed to optimize the four-pixel CIS structure. The results demonstrate how our stacked hybrid device could be the starting point for new device strategies in image sensor architectures. Furthermore, we expect the proposed approach to be applicable to a wide range of micro- and nanoelectronic devices and systems.

KEYWORDS: amorphous oxide semiconductor • In−Ga−Zn−O • image sensor • thin film transistor • nanometer scale • low-frequency noise

INTRODUCTION

Thin-film transistors (TFTs) have become indispensable components of various electronic/photonic devices used in daily life, such as computers, displays, healthcare appliances, mobile electronics, and sensors. Among the various semiconductor materials (1−9), active oxide semiconductors have been attracting steadily increasing attention as promising candidates for the next generation of TFTs (10) thanks to their low-temperature process capability (1−3, 11) and optical transparency. In particular, the amorphous In−Ga−Zn−O (*a*-IGZO) thin film is a well-known n-type oxide semiconductor that contains post-transition-metal cations with the outer s-orbitals overlapping and it exhibits high electron Hall mobility similar to that of crystalline structures (1, 2). More importantly, it offers the possibility of fabricating high mobility TFTs at room temperature (1, 2). Thus far, research efforts have been focused on the implementation of oxide TFTs with gate lengths of a few micrometers for display applications (11, 12). At the same time, little is known about the use of nanometer-scale oxide TFTs in analog/digital semiconductor device. By exploiting the aforementioned advantages of oxide TFTs, their possible applicability can extend to nondisplay applications (13).

Over the past decade, the complementary metal-oxide semiconductor (CMOS) image sensor technology has made notable advances. The challenge of further increasing the resolution of CMOS image sensors (CISs) by shrinking the pixel has been a major driving force for the overall advancement of imaging technology as a whole (14). Nonetheless, the pixel performance is inversely proportional to the pixel size of CIS. At a pace which can counteract the loss of performance as the pixels shrink, a number of new techniques have been introduced, such as back-side illumination, and light guide-waves placed on top of the pixels to improve the light sensitivity of imaging sensors (14, 15) (see Supporting Information 1). Still, there is consensus on the need for innovative technology allowing the realization of extremely small pixels, as the evolution of conventional Si-based CIS devices will soon reach the end of the roadmap because of inherent constraints. Recently, hybrid device approaches have been considered to provide the means to overcome fundamental limitations of current semiconductor devices (16−20). In this paper, we propose a hybrid CIS architecture combining nanometer-scale amorphous oxide TFTs with a conventional silicon photo diode (PD). This alternative approach to the fabrication of CIS devices is expected to open an avenue to continue down-scaling for

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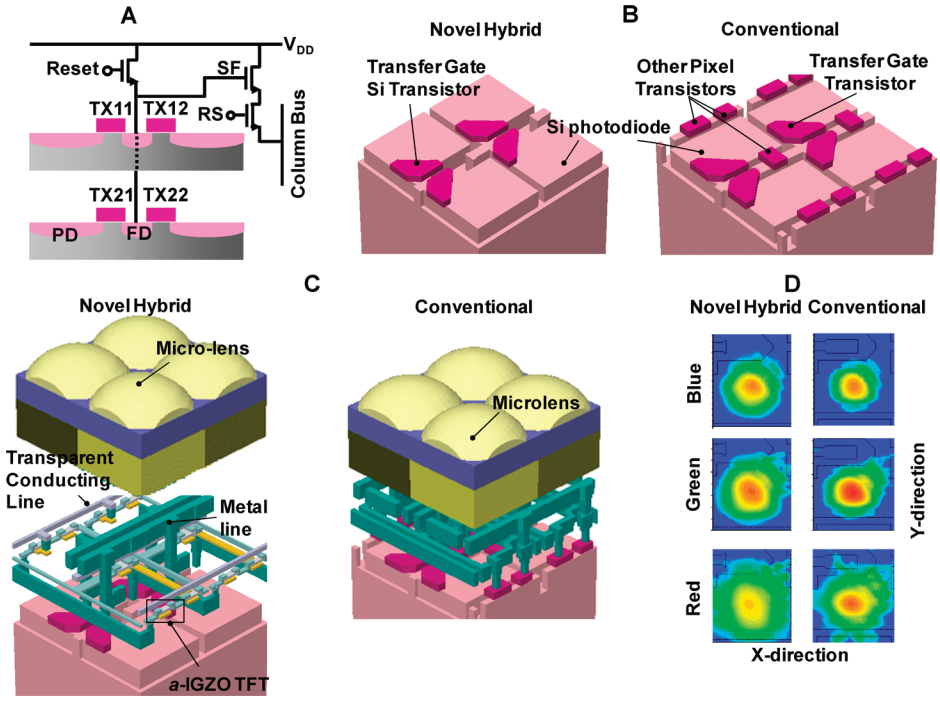

FIGURE 1. Novel hybrid CIS structure based on a combination of *a*-IGZO TFTs and a conventional CIS device. (A) Concept of a shared pixel circuit for a conventional CIS device. A group of 2 × 2 pixels shares the same output circuitry, including the source follower (SF), reset transistor (RES), row select (RS) transistor, and read out node. The cluster of pixels consists of four pinned photodiodes (PDs), four transfer gates (TXs) and two floating diodes (FDs). (B) First layer of the proposed novel hybrid and conventional four-pixel CIS structures generated using Sentaurus process simulator of Synopsys Co. Specifically, the first layer of the novel hybrid CIS device is composed of a Si PD (of light magenta color) and the TX (of pink color), while that of conventional CIS devices consists of a Si PD (of light magenta color) and all pixel transistors, including the TX transistor (of pink color) (C) Overview of novel hybrid CIS structure and a conventional CIS device. The second layer of the novel hybrid four-pixel CIS structure consists of interconnect metal lines and other pixel transistors based on *a*-IGZO TFTs (the RES transistor, the RS address transistor, and the SF transistor). The micro lenses are placed on top of the pixel structure to focus light onto the active Si substrate. (D) Electromagnetic power density contour plots for the novel hybrid structure and conventional CIS devices, which have been calculated by the Sentaurus electromagnetic solver. For comparisons between the performances of these two types of CIS devices, the electromagnetic power density of the blue pixel under blue light illumination, the green pixel under green light illumination, and the red pixel under red light illumination are shown.

several future generations when it would not be possible to further scale down conventional Si-based devices as shown in Figure S1 in Supporting Information. In addition, our research demonstrates the remarkably superior performance of short-channel oxide TFTs, their unique property of manageable flicker noise, and the excellent source-follower gain promised with significant potential for myriad micro- and nanoelectronic devices and systems. Lastly, we present the results of an extensive study on interface engineering in advanced materials such as those used for the fabrication of amorphous oxide TFT, including the formation of trapezoidal active channel, an Ar-plasma-induced In-rich IGZO surface, and the role of the SiO_2 interfacial layer, in the performance of short-channel devices, which was elucidated through chemical, structural, and electrical analyses.

EXPERIMENTAL SECTION

Materials. The concentration of gallium (Ga), indium (In), and zinc (Zn) in the amorphous oxide semiconductor, *a*-IGZO, on which the fabrication of the TFT was based, were determined by inductively coupled plasma-atomic emission spectrometry (ICP-AES) using the Shimadzu ICPS-8100 sequential spectrometer. It was found that the ratios of In/(Zn+Ga+In), Ga/(Zn+Ga+In), and Zn/(Zn+Ga+In) were 0.176, 0.391, and 0.433, respectively. X-ray diffraction data for IGZO revealed that a broad peak associated with the amorphous structure could be observed at temperatures as high as 600 °C. Further details of the materials employed for the fabrication of the *a*-IGZO TFT are presented in the Supporting Information.

Device Fabrication. A self-aligned top gate *a*-IGZO TFT was fabricated by a conventional semiconductor processing techniques at a temperature of less than 200 °C. More specifically, a reactive sputtering method was used to deposit the *a*-IGZO semiconductor active layer on a SiO_2/Si wafer (of 8-in. diameter) in a mixed Ar/O_2 atmosphere at room temperature. Nanometer-scale active regions were patterned by KrF photoresist on an antireflective coating layer using a leading-edge KrF scanner (Nikon NSR-S203B). The trapezoidal active channel was defined by an elaborate dry etch process (Oxford ICP380) in which the gas mixture used contained Ar and Cl_2 and the dry etching power was set to 300W. Prior to gate dielectric deposition, N_2O plasma treatment was carried out using plasma-enhanced chemical vapor deposition (PECVD,UNAXIS Co. SLR-7300) in a N_2O-rich atmosphere at a temperature of 150 °C. The role of the N_2O plasma treatment in the formation of *a*-IGZO semiconductor active layer is explained in detail in the Supporting

Information. As an interfacial dielectric layer, 25 Å-thick SiO_2 layer was deposited by PECVD (UNAXIS Co. SLR-7300) in a mixed SiH_4/N_2O atmosphere at a temperature of 150 °C. Our next step was to prepare a thin Al_2O_3 film at a temperature of 200 °C by radio frequency atomic layer deposition (ULVAC Co.) using a trimethylaluminum precursor as the Al source and ozone gas as oxidant. Subsequently, 100 nm thick Mo gate electrode was first deposited by DC sputtering in an Ar-rich atmosphere and then patterned by the above-mentioned KrF photolithography tool. For the formation of the self-aligned top gate structure, a unpatterned Mo region and a SiO_2/Al_2O_3 gate dielectric were successively etched by dry etching (Lam Co., TCP9400) with a gas mixture consisting of Cl_2 and O_2 and the dry etching power set to 100 W. To obtain source/drain regions of relatively low resistance, we carried out Ar plasma treatment on the exposed surface of the IGZO thin film. Upon its exposure to the Ar plasma, the resistivity of the IGZO thin film decreased considerably by approximately 5 orders of magnitude from 1×10^4 Ω cm to 4.0×10^{-1} Ω cm because of the presence of the In-rich surface. In addition, a 200 nm thick SiO_2 passivation layer was deposited by PECVD and contact holes were formed by dry etching (TEL SCCM) with a gas mixture consisting of CHF_3, CF_4, and Ar and dry etching power set to 1400 W. Finally, a Mo contact layer was formed by the aforementioned sputtering method, the same KrF photolithography tool, and dry etching process. Further details and schematics of the individual procedures adopted for the fabrication of each component of the *a*-IGZO TFT are presented in the Supporting Information.

General Electrical Analysis. The transfer and output characteristics of the *a*-IGZO TFT fabricated were evaluated on a customized probe station with the use of a Keithley 4200 system. The threshold voltage, V_T, was defined by the gate voltage, that induced a drain current of $W/L \times 10$ nA at a V_{DS} of 1.1 V. Information about the saturation mobility, μ_{sat}, in the *a*-IGZO TFT was extracted from postpinch-off data. As a consequence, problems associated with contact and other series resistance effects can be minimized. An estimate of the μ_{sat} was obtained from the slope of the straight line section of the $I_{DS}^{0.5}$ versus $(V_{GS}-V_T)$ curve and the following equation

$$\mu_{sat} = \frac{2m^2}{\frac{W}{L}C_g}$$

where m is $(I_{DS}^{0.5}/V_{GS}-V_T)$, W and L are the channel width and length, respectively, and C_g is the dielectric capacitance. Details about the results of the electrical analysis based on conductance method and flicker noise measurements are presented in the Supporting Information.

RESULTS AND DISCUSSION

Figure 1A shows the concept of a shared pixel circuit for a CIS device. Details about the operating principle of CIS device are presented in Supporting Information 2. A group of 2 × 2 pixels shares the same output circuitry including the source follower (SF), the reset transistor (RES), the row select (RS) transistor and the read-out node. Next to the listed components, the cluster of pixels consists of four pinned PDs, four transfer gates (TX), and two floating diodes (FDs). This structure provides the benefit of reducing the number of transistors and interconnections per pixel. However, to realize image pixels with a pitch of 1.4 μm and beyond, the pixels need to be scaled down further. However, down-scaling results in loss of the fill factor because of the shrinkage of the PD areas. In the proposed stacked CIS architecture, we successfully enlarged the PD area within the active region that is occupied by the PD through a different approach involving a stack device architecture. Figure 1B obtained by the Sentaurus process simulator (Synopsys Co.) shows only the first layer of the four-pixel CIS structure. This layer is composed of the silicon PD and the TX transistor, which requires a relatively low leakage current flowing through the floating diode, whereas that of a conventional CIS device consists of a silicon PD and all pixel transistors. As seen in Figure 1C, owing to the *a*-IGZO TFTs being stacked, pixel transistors such as the (SF, RES, RS) were laid on top of the interconnect metal lines in the proposed hybrid CIS architecture. As a result, the area within the active region occupied by the Si PD can be effectively enlarged. Some interconnect metal lines employed for delivering constant voltage, V_{DD}, have also been replaced with a transparent conducting oxide (TCO) allowing the reduction of light scattering and an increase in the fill factor. In addition, microlenses have been placed on top of the pixel structure to focus light between the interconnect metal lines, avoiding unwanted light scattering and crosstalk while maximizing the detector's efficiency. To compare the performance of conventional CIS devices and the novel hybrid CIS, we performed 3D optical simulations. As shown in Figure 1D, as compared to conventional devices, the novel hybrid CIS shows enlarged power contours for subpixels at blue, green and red wavelengths. Even if the parameters such as the distance between the microlens and the active region have been optimized on the basis of the structure of conventional CIS devices, the simulation results reveals a quantum efficiency increase of 143, 116, and 120% at blue, green, and red wavelengths, respectively. The improved performance of the novel hybrid CIS device was attributed to the significantly enlarged PD area and implementation of TCO interconnect lines (see Figure S3 in the Supporting Information). It should be noted that the proposed architecture offers further advantage in terms of pixel optimization and performance as pixels become smaller and electrical crosstalk increases. In addition, further improvements are possible by employing back side illumination with novel hybrid CIS devices.

To utilize oxide TFTs for high-density CISs with relatively small pixels, it is necessary to have nanometer-scale TFTs that ensure good short channel immunity, manageable flicker noise (1/*f* noise), and acceptable source-follower gain. Figure 2 shows the structure as well as electrical character-

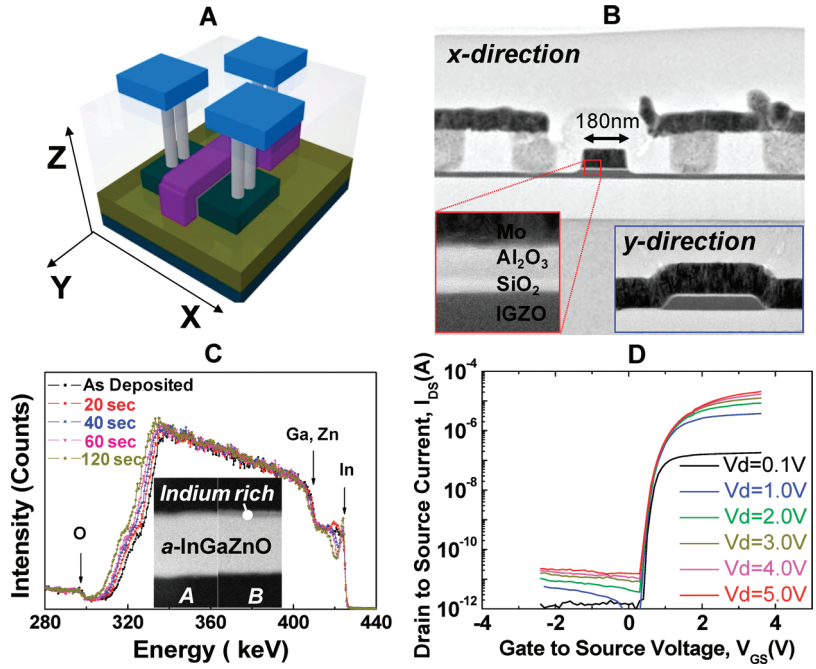

FIGURE 2. Structure and electrical characteristics of *a*-IGZO TFT with gate length of nanometer scale. (A) Schematic diagram of self-aligned top gate *a*-IGZO TFT. (B) Cross-sectional transmission electron microscope (TEM) image of *a*-IGZO TFT with gate length of 180 nm taken along the *x*-direction of Figure 2A. The inset on the bottom left side shows an enlarged image of the *a*-IGZO TFT, revealing that the gate stack is composed of a dual gate dielectric layer of Al_2O_3/SiO_2. The inset on the bottom right side shows a TEM image taken along the y-direction of Figure 2A. The trapezoidal IGZO active structure can be identified on top of the SiO_2 isolation layer. The width of the bottom and top active regions are 250 nm, and 200 nm, respectively. (C) Rutherford backscattering spectra of different chemical elements as a function of duration of the Ar plasma treatment. The inset shows high-resolution TEM images of a *a*-IGZO thin film (a) before and (b) after the Ar plasma treatment. It is worth noting that after the Ar plasma treatment of the *a*-IGZO thin film, an IGZO region with comparatively high carrier concentration (n+) is formed because of the In-rich region formed on top of the IGZO film. (D) $I_{DS}-V_{GS}$ transfer characteristics with increasing V_{DS} from 0.1 to 5.0 V in steps of ~1.0 V.

istics of a *a*-IGZO TFT with nanometer scale gate length. Specifically, Figure 2A shows a schematic drawing of the self-aligned top gate *a*-IGZO TFT. As depicted in Figure 2B, the cross-sectional transmission electron microscopy (TEM) image reveals 180 nm gate length *a*-IGZO TFT having a top gate structure, dual gate dielectric layer (Al_2O_3/SiO_2), and trapezoidal active region. The self-aligned top gate structure was employed to achieve low parasitic capacitance and good scalability (21). For the realization of a nanometer-scale *a*-IGZO TFT with improved performance, we introduced both a high-κ dielectric and a trapezoidal active channel. High-κ gate dielectric affords high capacitance, which in turn allows more efficient charge injection into the channels with comparatively low leakage current (22, 23). In general, a multi channel transistor structure offers improvements in the channel performances mainly because the increase in the gate width results in an improved performance of transistor while retaining the short gate length (24). In the set of experiments performed, the trapezoidal active region was defined through a tailored dry etching process. The trichannel structure with rounded corners obtained was also characterized by excellent short-channel performance, as illustrated in Figure 2D. The formation of trichannel structures can, however, be avoided because the enhanced electric field through the sharp edge corners may result in significant leakage current across the low-temperature processed gate dielectric, thereby leading to failure of the transistor operation. In addition, in the case of a high-performance short-channel device, lowering the series resistance between electrodes and the IGZO channel region is essential. To this end, Ar plasma treatment was carried out during the fabrication of the *a*-IGZO TFT. Upon its exposure to the Ar plasma on IGZO surface, the resistivity of the IGZO thin film decreased by approximately 5 orders of magnitude from 1×10^4 Ω cm to 4.0×10^{-1} Ω cm. Figure 2C shows the Rutherford backscattering spectrum of different chemical elements as a function of the duration of the Ar plasma treatment. In the case of an exposure time ranging between 20 and 40s, the In peak is separated into two regions. As can seen in the inset, a 3 nm thick In-rich surface was formed on top of the IGZO thin film after Ar plasma treatment, which contributes to the formation of an IGZO region of a comparatively high carrier concentration (n^+) and the realization of an IGZO TFT with superior performance. Figure 2D shows the transfer characteristics of a 180 nm *a*-IGZO TFT with increasing V_{DS} from 0.1 V to 5.0 V in steps of 1.0 V. The saturation mobility induced at a relatively high drain bias (V_{DS} = 3.0 V) was determined. The fabricated 180 nm *a*-IGZO TFT with an equivalent oxide thickness of 5 nm (50 Å Al_2O_3/25 Å SiO_2) was characterized by a drive current of 100 μA/μm, a mobility of 18 $cm^2\ eV^{-1}\ s^{-1}$, a subthreshold slope as low as 70 mV/dec, a negligible drain induced barrier lowering (DIBL) of 20 mV/V, an I_{on}/I_{off} modulation ratio of ~1×10^6, and a positive threshold voltage of 0.6 V. It should be noted that these values are all superior to the previous reported characteristics of subμm oxide TFTs (12−14, 25).

To achieve the high performance of the *a*-IGZO TFT proposed in this paper, various optimization processes with

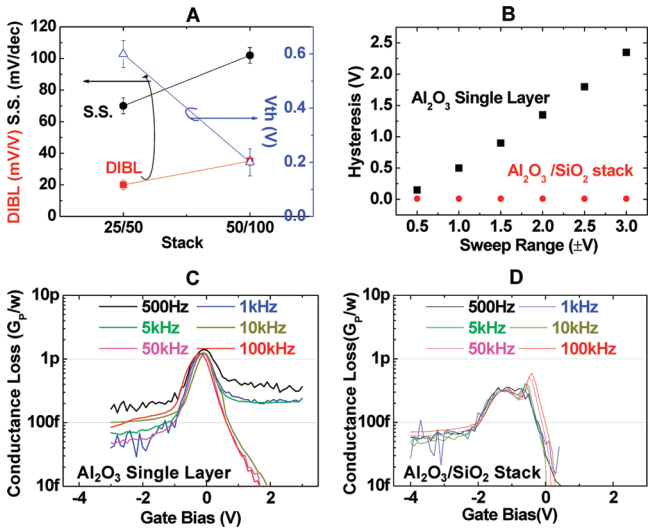

FIGURE 3. Influence of gate stack thickness on the electrical characteristics of *a*-IGZO TFT. (A) Threshold voltage, subthreshold slope, and drain induced barrier lowering (DIBL) of a *a*-IGZO TFT with a 180 nm gate length, 50 Å thick Al_2O_3/25 Å thick SiO_2, and 100 Å thick Al_2O_3/50 Å-thick SiO_2 gate dielectrics. (B) Hysteresis versus charge trapping for an MOS capacitor with a single Al_2O_3 gate dielectric and an Al_2O_3/SiO_2 dual stack structure. (C) Frequency-dependent conductance loss versus gate voltage for a MOS capacitor with a single Al_2O_3 gate dielectric and an *a*-IGZO semiconductor. (D) Frequency-dependent conductance loss versus gate voltage for a MOS capacitor with Al_2O_3/SiO_2 dual gate dielectric and a *a*-IGZO semiconductor.

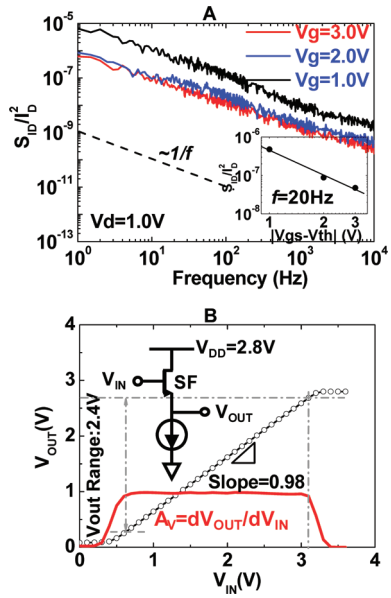

FIGURE 4. Low-frequency noise behavior and SF performance of *a*-IGZO TFT with W/L=180 nm/250 nm. (A) Normalized drain−current noise power spectral density (S_{ID}/I_D^2) versus frequency with V_{GS} increasing from 1.0 to 3.0 V and for a constant V_{DS} of 1.0 V. The inset shows the normalized S_{ID}/I_D^2 versus the gate voltage overdrive $|V_{GS}-V_{th}|$ at a frequency of 20 Hz. (B) V_{OUT} versus V_{IN} of a SF-based *a*-IGZO TFT with W/L=180 nm/250 nm. The red line indicates the derivative of V_{OUT} with respect to V_{IN}. The inset shows the circuit schematics of the SF at a V_{DD} of 2.8 V.

respect to the gate stack were carried out, as shown in Figure 3. More specifically, Figure 3A shows the influence of gate stack thickness on the performance of the *a*-IGZO TFT with a drain current of W/L=180 nm/250 nm. As expected, a relatively thick gate dielectric results in rapid deterioration of the performance of the short channel device including a decrease in the threshold voltage, and an increase in the DIBL as well as the subthreshold slope. Thus the employment of a thin gate stack and high-κ dielectric is a sensible strategy for further downscaling of the *a*-IGZO TFT below 100 nm. As shown in Figure 3B, a MOS capacitor with a single Al_2O_3 gate dielectric suffers from severe charge trapping, whereas a MOS device with an Al_2O_3/SiO_2 dual stack structure exhibits negligible hysteresis (Figure 3b). On the other hand, Figures 3C and 3D show the effects of the interfacial SiO_2 layer on the conductance loss of *a*-IGZO semiconductor-based MOS capacitors. The ac conductance method is widely considered as the most accurate way of determining the interface trap density (D_{it}) (see Supporting Information 7). With the use of this method, it was revealed that the interfacial SiO_2 layer between Al_2O_3 and *a*-IGZO significant affects the overall interface quality. Compared to a MOS capacitor with a single Al_2O_3 dielectric, a MOS device with an Al_2O_3/SiO_2 dual stack structure shows a relatively low conductance loss peak, which in turn indicates low D_{it} (26). This behavior can be attributed to the interfacial SiO_2 layer that prevents the formation of an Al-IGZO electrically active interfacial layer, between IGZO and Al_2O_3, and it has been verified by energy dispersive spectroscopy analysis as presented in Supporting Information 8. Therefore, to be able to integrate a high-κ Al_2O_3 layer into the *a*-IGZO semiconductor-based TFTs, the interfacial SiO_2 layer should lower both the interface state density and the charge trapping.

Among the various pixel transistors of a CIS, the voltage-amplifying SF transistor should meet stringent requirements of low frequency (*f*) noise and power consumption. Thus, before *a*-IGZO TFTs can be integrated into pixel transistors, a manageable low *f* noise behavior and acceptable SF performance (e.g., output gain and V_{OUT} range) of these oxide semiconductor-based TFTs should be addressed. Figure 4 shows the low *f* noise behavior and SF performance of a *a*-IGZO TFT with a drain current of W/L = 180 nm/250 nm. As seen in Figure 4A, the normalized drain-current noise spectral density (S_{ID}/I_D) fits well to the inverse power low: $1/f^{\gamma}$, with $\gamma \approx 1$ in all V_{DS} bias conditions, which indicates that the low *f* noise behavior of an a-IGZO TFT with 180 nm gate length also obeys the classical $1/f$ noise theory (27). The inset of Figure 4A shows the normalized S_{ID}/I_D dependence of the gate voltage overdrive $|V_{GS} - V_{th}|$ at 20 Hz. More specifically, the normalized S_{ID}/I_D varies as $(V_{GS} - V_{th})^{-m}$ with $m \approx 2.0$, which highlighting the fact that noise is mainly due to fluctuation in the carrier number (Δn) caused by the tunneling of free-charge carriers into oxide traps close to the SiO_2-*a*-IGZO interface (27, 28). As a figure of merit in assessing the noise level, Hooge's parameter, α_H, is extracted and evaluated to be in the range of $2-3 \times 10^{-3}$ at ($V_{GS}-V_{th} > V_D$) (see Supporting Information 9), i.e., close to that of n-MOSFET devices with high-κ dielectrics (27, 28).

On the other hand, the SF gain (A_V) was experimentally obtained through the first derivative of V_{OUT} with respect to V_{IN} and the results are presented in Figure 4B. The A_V value of the fabricated *a*-IGZO TFT was found to be 0.98, which is

close to theoretical limit. The remarkable SF gain can be explained by the following eqs 1 and 2 (29, 30).

$$A_V = \frac{dV_{OUT}}{dV_{IN}} = \frac{g_m}{ng_m + g_D} \quad (1)$$

$$n = 1 + \alpha \text{ with } \alpha = \frac{C_{CH\text{-}GND}}{C_{G\text{-}CH}} \quad (2)$$

where n denotes the body factor; g_m, the transconductance; $g_{D,}$ the output drain conductance; $C_{CH\text{-}GND}$, the capacitance between the channel and ground (the back gate in the case of silicon-on-insulator devices or the substrate in the case of bulk devices); and $C_{G\text{-}CH}$, the capacitance between the gate and the channel. In the case of a bulk transistor, typical values for n range between 1.3 and 1.5 and between 1.05 and 1.1 in the case of fully depleted (FD) silicon on insulator MOS field-effect transistor (29, 30). Because we used a wide-bandgap semiconductor on a 200 nm thick SiO_2 insulator, negligible impact ionization combined with a relatively low α value (0.025) resulted in a reduced g_D and a low n of 1.025, respectively. The combination of these characteristics resulted in a remarkable SF gain of 0.98 and V_{OUT} range of 2.4 V.

CONCLUSION

In this paper, we propose a novel hybrid CIS architecture based on oxide TFTs with gate length of nanometer scale, which demonstrates excellent device performance, rendering it ideal for future high-density image sensor applications. Specifically, *a*-IGZO TFTs with a gate length of 180 nm fabricated at a temperature less than 200 °C show excellent short channel performance, manageable low $1/f$ noise, and outstanding SF output gain. In conclusion, the scalability of a-IGZO TFTs to down to nanometer scale suggests that these oxide TFTs can be considered as promising candidates for switch elements of high density CIS devices. On the basis of their low-temperature stackable nature, optical transparency, and excellent short channel performance demonstrated in this study, the first decisive steps toward achieving a workable high-density CIS with unprecedented small pixel size, well beyond the extrapolations of the conventional Si-based solutions, are expected to be made in the near future

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Supporting Information Available: Additional figures (PDF). This materials is available free of charge via the Internet at http://pubs.acs.org.

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